

Formation Automatique et Informatique Industrielle

Master 1 S2

Matière : Systèmes Embarqués et Systèmes
Temps Réel SE-STR

Par : ATOUI Hamza

Plan du cours

- Le μ C PIC16F84A :
 - Principales caractéristiques.
 - Brochage.
 - Synoptique & architecture interne du PIC16F84A.
 - Mot de configuration & configuration de l'oscillateur.
 - Organisation de l'espace DATA/IO & FLASH CODE.
 - Registres Spéciaux.

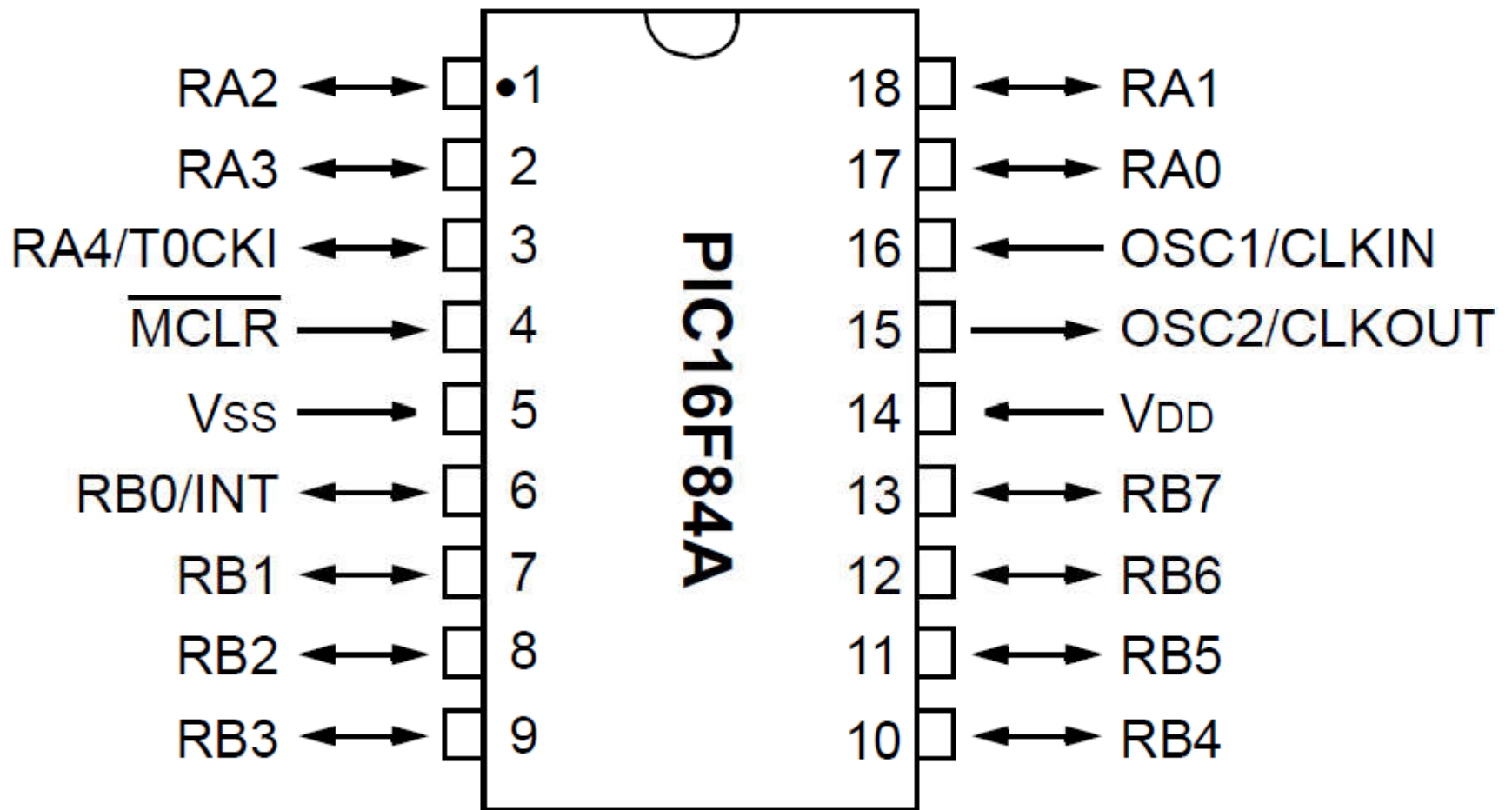
Le PIC16F84A

- Pour quoi on va commencer par l'étude de PIC16F84A, pour quoi pas d'autre dans la même famille 16Fxxx ???

Principales caractéristiques

- Le PIC16F84A est un μ C de la série 16Fxxx équipé par le μ P MID-RANGE, et des fonctionnalités I/O qui permettent de réaliser des montages avec un minimum de composants externes.
- Les caractéristiques de PIC16F84A:
 - 2 ports I/O (PORTA : 5 lignes, PORTB : 8 lignes).
 - TIMER 8 bits.
 - EEPROM de 64 octets.
 - Un chien de garde (WDT).
 - Mémoire programme FLASH de 1Kx14bits.
 - RAM de 68 octets.
 - Compatible avec les PIC16CR84, PIC16C84 et PIC16F84.

Brochage

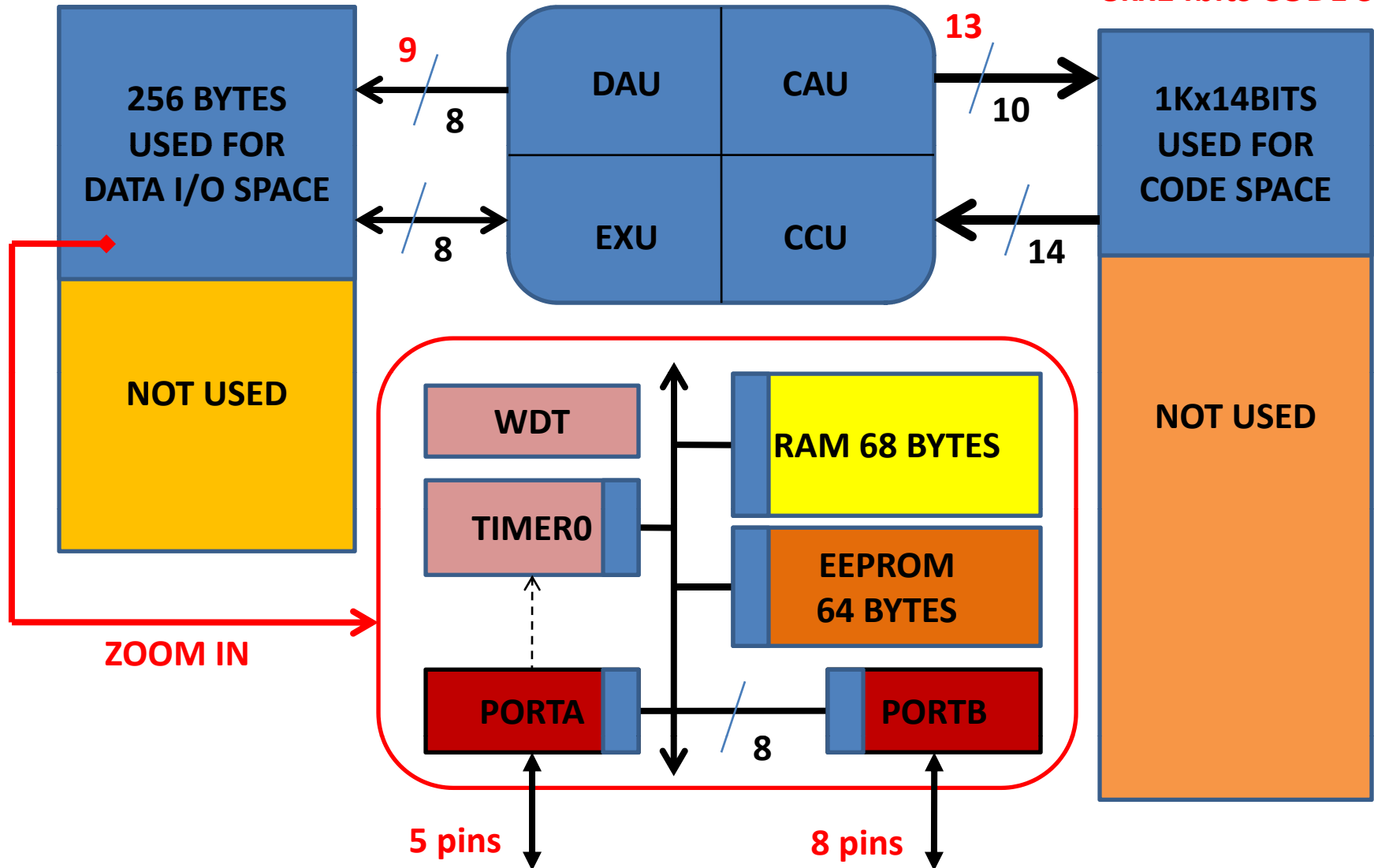


Projection de PIC16F84A sur le MID-RANGE

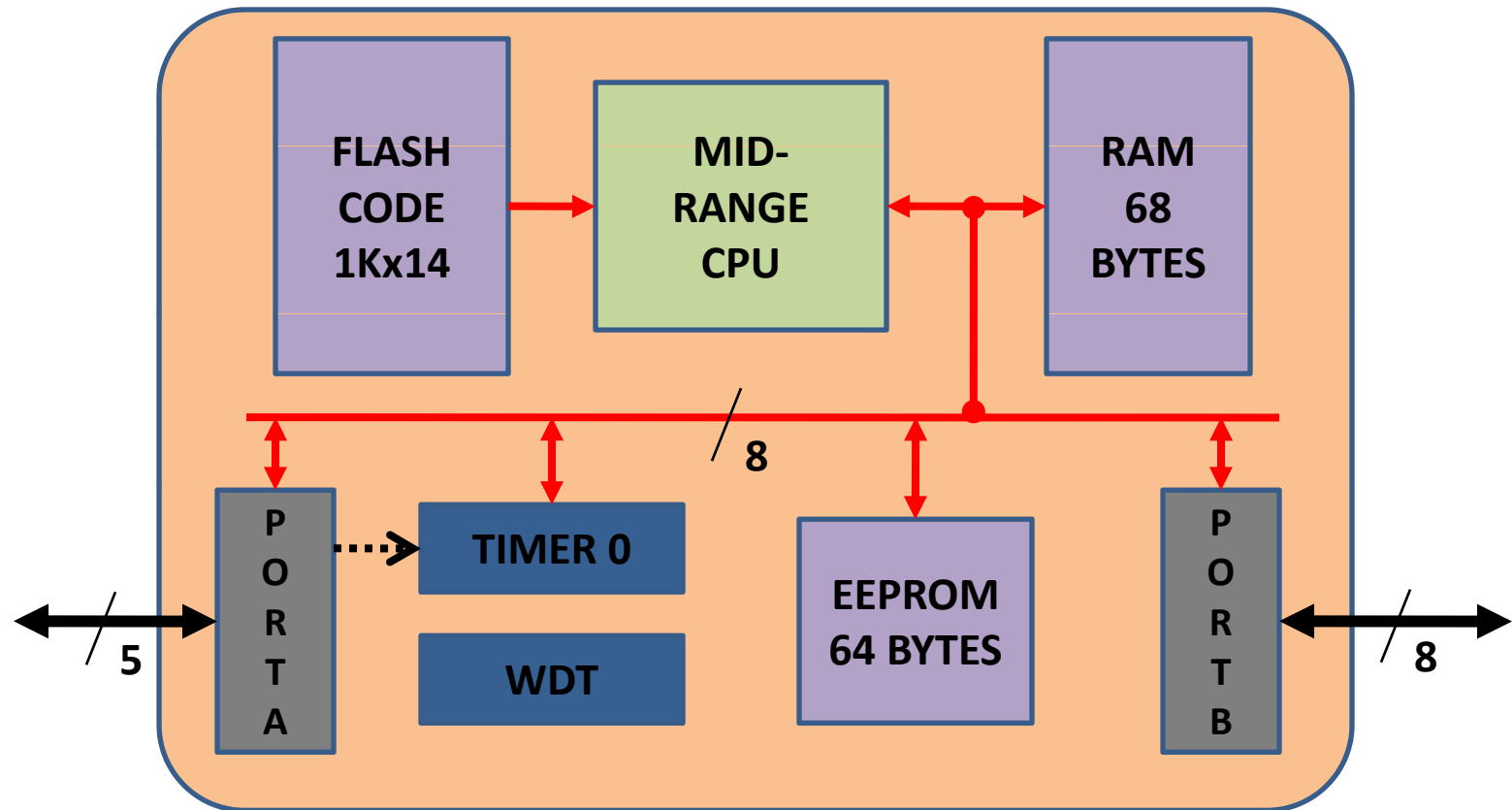
512x8bits DATA/IO SPACE

MID-RANGE μ P

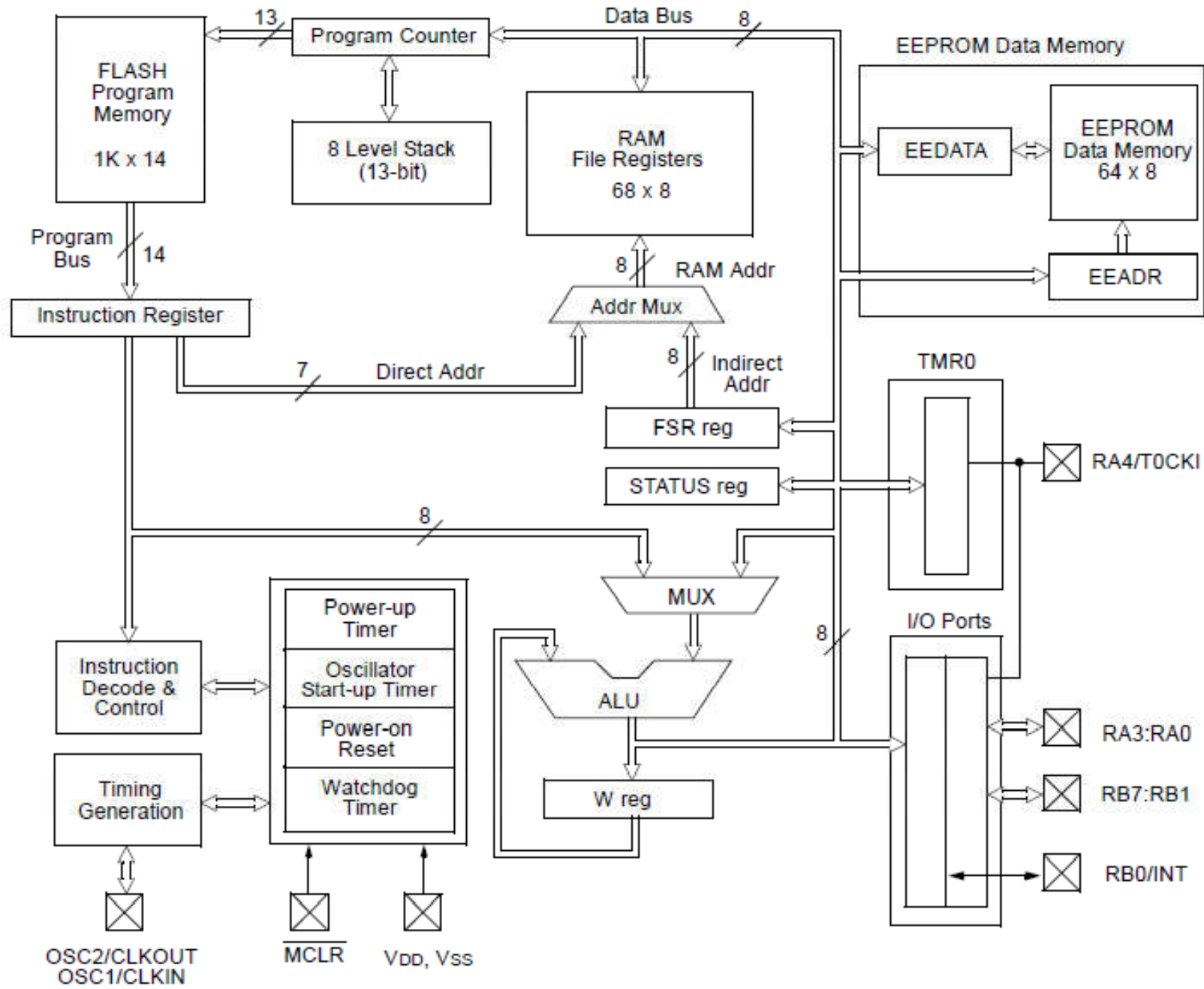
8Kx14bits CODE SPACE



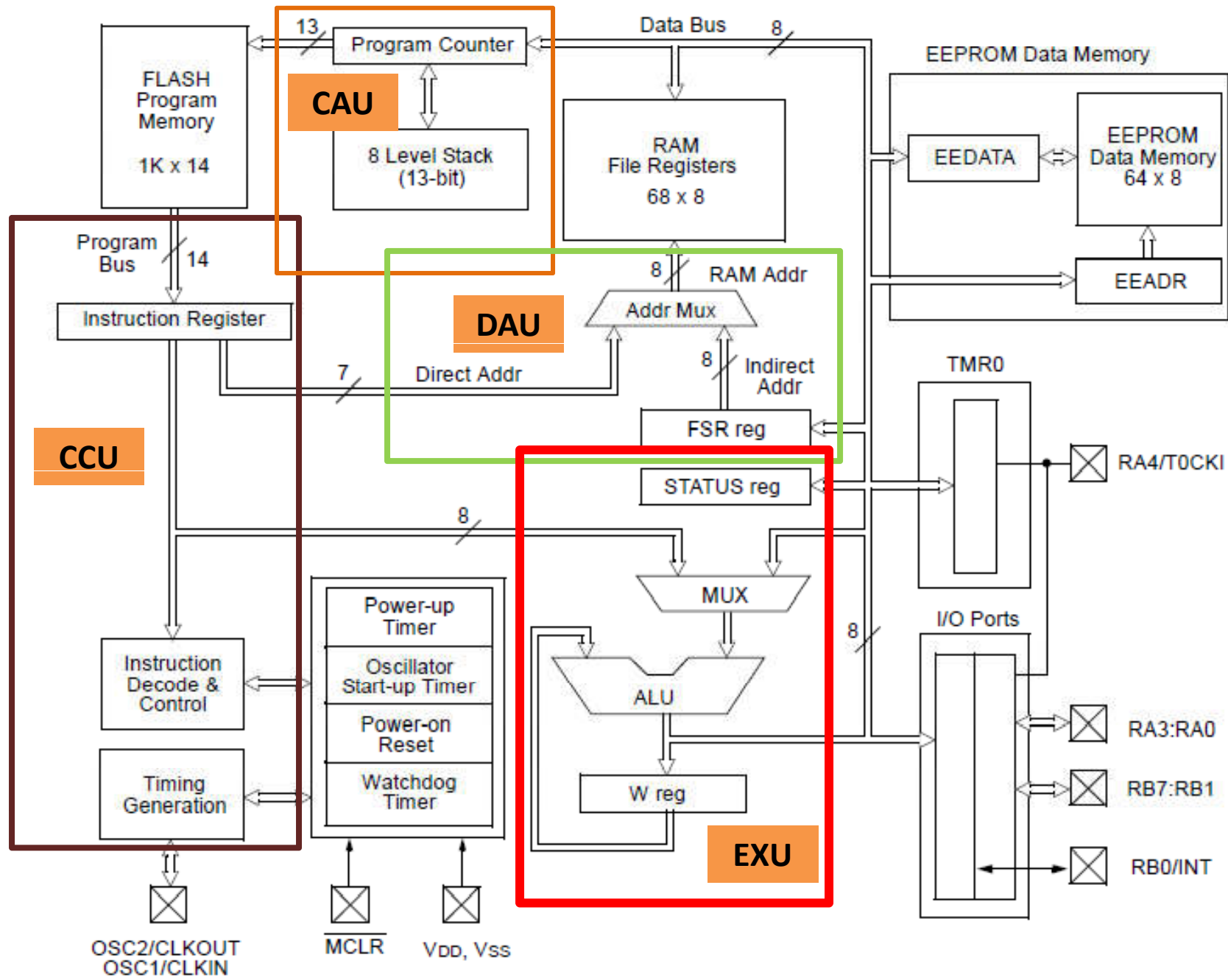
Synoptique & architecture interne du PIC16F84A



Architecture Interne d'après le DATASHEET !!!???



Architecture Interne d'après le DATASHEET



Mot de configuration & configuration de l'oscillateur

- Le mot de configuration est implémenté à l'adresse 2007h pour configurer:
 - La protection de la zone FLASH CODE.
 - Activation du TIMER de démarrage.
 - Activation du WDT.
 - Sélection de l'oscillateur.

PIC16F84A CONFIGURATION WORD

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	PWRT $\overline{\text{E}}$	WDTE	F0SC1	F0SC0
bit13											bit0		

bit 13-4 **CP:** Code Protection bit
 1 = Code protection disabled
 0 = All program memory is code protected

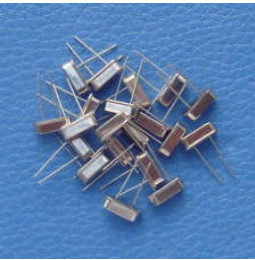
bit 3 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
 1 = Power-up Timer is disabled
 0 = Power-up Timer is enabled

bit 2 **WDTE:** Watchdog Timer Enable bit
 1 = WDT enabled
 0 = WDT disabled

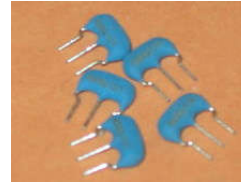
bit 1-0 **F0SC1:F0SC0:** Oscillator Selection bits
 11 = RC oscillator
 10 = HS oscillator
 01 = XT oscillator
 00 = LP oscillator

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

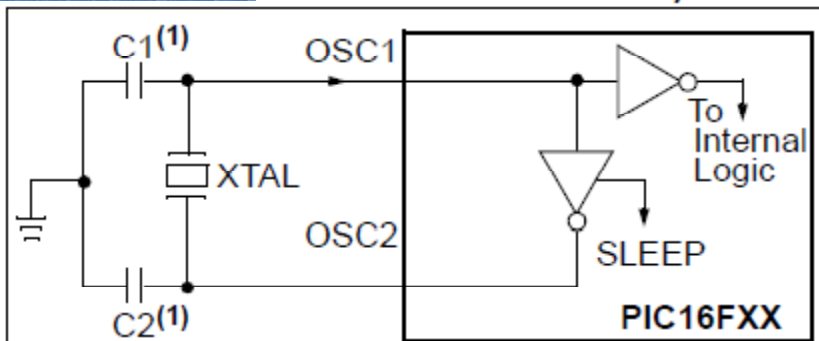
Mot de configuration & configuration de l'oscillateur



CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



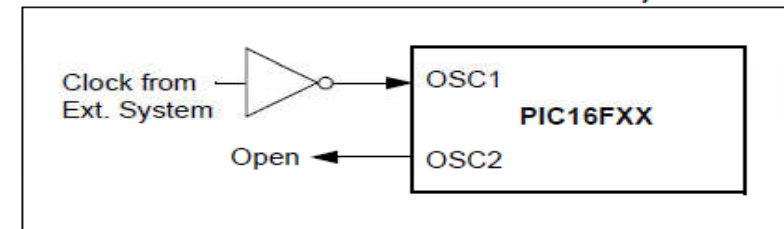
EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



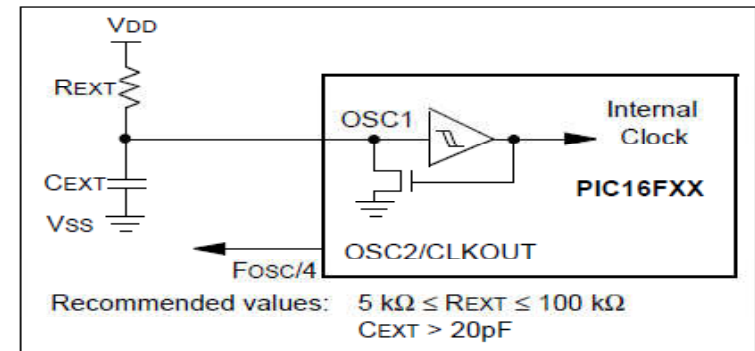
Note 1: See Table 6-1 for recommended values of C1 and C2.

CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	20 MHz	15 - 33 pF	15 - 33 pF



RC OSCILLATOR MODE



The frequency of such oscillator is calculated according to the formula $f = 1/T$ in which:

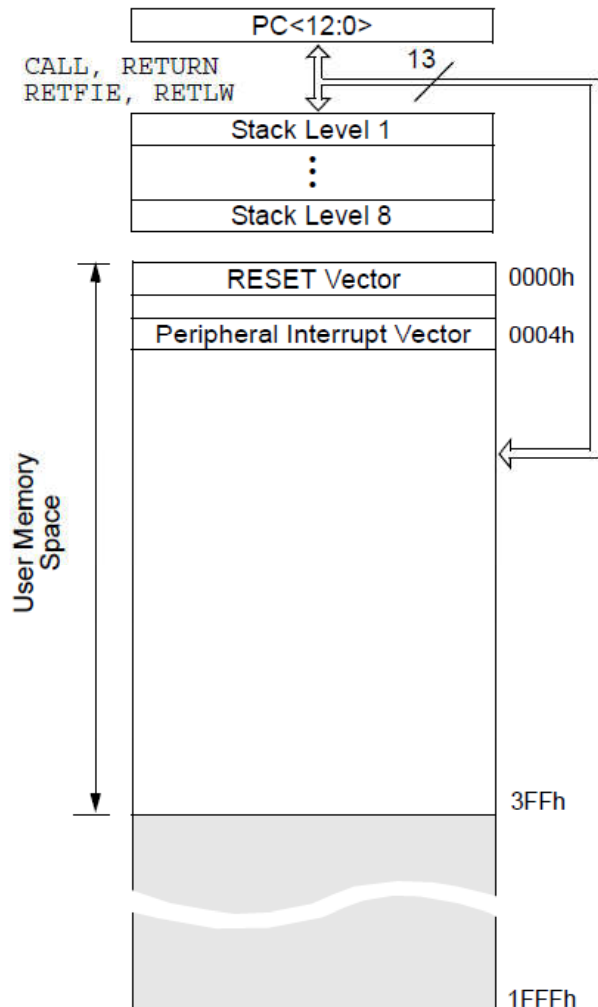
f = frequency [Hz]

$T = R * C$ = time constant [s]

R = resistor resistance [Ω]

C = capacitor capacity [F]

Organisation de l'espace DATA/IO & FLASH CODE

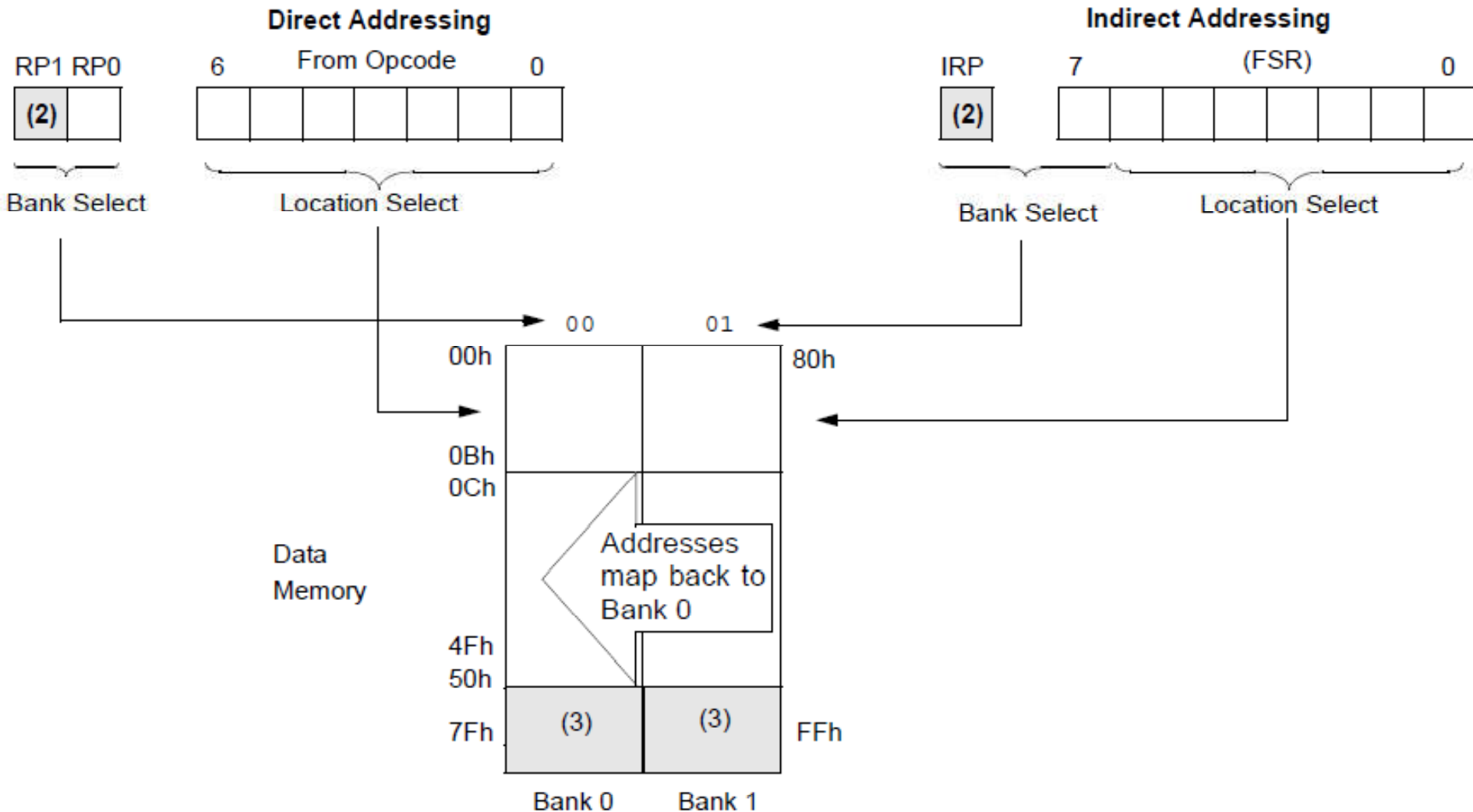


Registres internes de MID-RANGE

File Address		File Address
00h	Indirect addr. ⁽¹⁾	80h
01h	TMR0	81h
02h	PCL	82h
03h	STATUS	83h
04h	FSR	84h
05h	PORTA	85h
06h	PORTB	86h
07h	—	87h
08h	EEDATA	88h
09h	EEADR	89h
0Ah	PCLATH	8Ah
0Bh	INTCON	8Bh
0Ch		8Ch
	68 General Purpose Registers (SRAM)	
	Mapped (accesses) in Bank 0	???
4Fh		CFh
50h		D0h
7Fh		FFh
	Bank 0	Bank 1

Unimplemented data memory location, read as '0'.
Note 1: Not a physical register.

ADDRESSING MODES



Note

2: Maintain as clear for upward compatibility with future products.

3: Not implemented.

Registres Spéciaux

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
Bank 0											
00h	INDF	Uses contents of FSR to address Data Memory (not a physical register)								---- --	11
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
02h	PCL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
03h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
04h	FSR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
05h	PORTA ⁽⁴⁾	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
06h	PORTB ⁽⁵⁾	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
07h	—	Unimplemented location, read as '0'								—	—
08h	EEDATA	EEPROM Data Register								xxxx xxxx	13,14
09h	EEADR	EEPROM Address Register								xxxx xxxx	13,14
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10
Bank 1											
80h	INDF	Uses Contents of FSR to address Data Memory (not a physical register)								---- --	11
81h	OPTION_REG	RBP1	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	11
83h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	11
85h	TRISA	—	—	—	PORTA Data Direction Register				---1 1111	16	
86h	TRISB	PORTB Data Direction Register								1111 1111	18
87h	—	Unimplemented location, read as '0'								—	—
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
89h	EECON2	EEPROM Control Register 2 (not a physical register)								---- --	14
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾				---0 0000	11	
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10

Legend: x = unknown, u = unchanged. - = unimplemented, read as '0', q = value depends on condition

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> are never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a MCLR Reset.

3: Other (non power-up) RESETS include: external RESET through MCLR and the Watchdog Timer Reset.

4: On any device RESET, these pins are configured as inputs.

5: This is the value that will be in the port output latch.